

* * * * * 2/11/96
=> s 174/52.1-52.4/cclst or 257/666,667,6
73,676,678,684,690,692,693,704,787,789/ccls or
361/760,772,773,816,818,829/ccls or 29/829,830,831,832,841,827,854,855/ccls o
437/209,220,224/ccls

3404 174/52.1-52.4/CCLST (4 TERMS)
(174/52.1+NEXT3/CCLST)

367 257/666/CCLS

62 257/667/CCLS

54 257/673/CCLS

276 257/676/CCLS

241 257/678/CCLS

72 257/684/CCLS

158 257/690/CCLS

200 257/692/CCLS

167 257/693/CCLS

171 257/704/CCLS

355 257/787/CCLS

18 257/789/CCLS

1705 257/666,667,673,676,678,684,690,692,693,704,787,789/CCLS

((257/666 OR 257/667 OR 257/673 OR 257/676 OR 257/678 OR

257 /684 OR 257/690 OR 257/692 OR 257/693 OR 257/704 OR 257/7

87 OR 257/789)/CCLS)

413 361/760/CCLS

220 361/772/CCLS

257 361/773/CCLS

290 361/816/CCLS

310 361/818/CCLS

151 361/829/CCLS

1531 361/760,772,773,816,818,829/CCLS

((361/760 OR 361/772 OR 361/773 OR 361/816 OR 361/818 OR

361 /829)/CCLS)

231 29/829/CCLS

366 29/830/CCLS

121 29/831/CCLS

382 29/832/CCLS

190 29/841/CCLS

458 29/827/CCLS

307 29/854/CCLS

77 29/855/CCLS

1968 29/829,830,831,832,841,827,854,855/CCLS

((29/829 OR 29/830 OR 29/831 OR 29/832 OR 29/841 OR 29/82

7 O R 29/854 OR 29/855)/CCLS)

814 437/209/CCLS

365 437/220/CCLS

77 437/224/CCLS

1126 437/209,220,224/CCLS

((437/209 OR 437/220 OR 437/224)/CCLS)

L1 8464 174/52.1-52.4/CCLST OR 257/666,667,673,676,678,684,690,692,

693 ,704,787,789/CCLS OR 361/760,772,773,816,818,829/CCLS OR 29

/82 9,830,831,832,841,827,854,855/CCLS OR 437/209,220,224/CCLS
=> s (((chip (w) package) or (chip (w) carrier) or (carrier (w) package) or

(integrated (w) circuit (w) device)) or (IC (w) device) or (semiconductor (w) package) or (SC (w) package) or (integrated (w) package) or (integrated (w) device))/ab)) and l1

UNMATCHED RIGHT PARENTHESIS '/AB))'

=> s (((chip (w) package) or (chip (w) carrier) or (carrier (w) package) or (integrated (w) circuit (w) device)) or (IC (w) device) or (semiconductor (w) package) or (SC (w) package) or (integrated (w) package) or (integrated (w) device))/ab) and l1

UNMATCHED RIGHT PARENTHESIS '/AB) AND'

YOU HAVE RECEIVED THIS ERROR MESSAGE 2 CONSECUTIVE TIMES

The number of right parentheses in a query must be equal to the number of left parentheses.

IF YOU REQUIRE FURTHER HELP, PLEASE CONTACT YOUR LOCAL HELP DESK

=> s (((chip (w) package) or (chip (w) carrier) or (carrier (w) package) or (integrated (w) circuit (w) device) or (IC (w) device) or (semiconductor (w) package) or (SC (w) package) or (integrated (w) package) or (integrated (w) device))/ab) and l1

9712 CHIP/AB

13279 PACKAGE/AB

99 CHIP (W) PACKAGE

9712 CHIP/AB

42594 CARRIER/AB

418 CHIP (W) CARRIER

42594 CARRIER/AB

13279 PACKAGE/AB

41 CARRIER (W) PACKAGE

24068 INTEGRATED/AB

145483 CIRCUIT/AB

252791 DEVICE/AB

938 INTEGRATED (W) CIRCUIT (W) DEVICE

2589 IC/AB

252791 DEVICE/AB

125 IC (W) DEVICE

33950 SEMICONDUCTOR/AB

13279 PACKAGE/AB

232 SEMICONDUCTOR (W) PACKAGE

466 SC/AB

13279 PACKAGE/AB

0 SC (W) PACKAGE

24068 INTEGRATED/AB

13279 PACKAGE/AB

12 INTEGRATED (W) PACKAGE

24068 INTEGRATED/AB

252791 DEVICE/AB

63 INTEGRATED (W) DEVICE

L2 356 (((CHIP (W) PACKAGE) OR (CHIP (W) CARRIER) OR (CARRIER (W)

PA

CKAGE) OR (INTEGRATED (W) CIRCUIT (W) DEVICE) OR (IC (W) DE

VIC

E) OR (SEMICONDUCTOR (W) PACKAGE) OR (SC (W) PACKAGE) OR (I

NTE

GRATED (W) PACKAGE) OR (INTEGRATED (W) DEVICE))/AB) AND L1

=> s (chip or die) and l2

74834 CHIP

89867 DIE

L3 336 (CHIP OR DIE) AND L2

=> s (lead#) and l3

438312 LEAD#

L4 296 (LEAD#) AND L3
=> s (housing#) and l4

372213 HOUSING#

L5 61 (HOUSING#) AND L4
=> s l4 not l5

L6 235 L4 NOT L5

=> save l6 leadframe/a

ANSWER SET 'L6' HAS BEEN SAVED AS 'LEADFRAME/A'

=> sor pn

SORT IS APPROXIMATELY 62% COMPLETE; ENTER 'END' TO CANCE